H-706-02

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Prior Application: J. ETOH et al
Serial No. 09/095,101
Filed: June 10, 1998

Group Art Unit: 2818
Examiner: S. Mai
For: LARGE SCALE INTEGRATED CIRCUIT WITH SENSE AMPLIFIER CIRCUITS FOR LOW VOLTAGE OPERATION

PRELIMINARY AMENDMENT

Assistant Commissioner of Patents
Washington, D.C. 20231

Sir:

Prior to examination, please amend the above-identified application as follows:

IN THE SPECIFICATION

Please amend the specification as set forth below.

Page 1, before the first line of the specification please insert the sentence:

This application is a continuation application of U.S. Serial No. 09/095,101, filed June 10, 1998.

IN THE CLAIMS

Cancel claims 1-52, and add new claims 53-74 as follows.

53. A semiconductor device comprising:

a circuit block including a first node and a second node for receiving an operating voltage and a plurality of complementary MISFETs, each having a p-channel MISFET and an n-channel MISFET connected in series between the first node and the second node,

wherein said semiconductor device has a first operation mode and a second operation mode,

wherein in the first operation mode, a first current between the first node and the second node flows through each of the plurality of complementary MISFETs when the voltage between the gate and the source of one of the p-channel MISFET and the n-channel MISFET is 0 volts for each of the plurality of complementary MISFETs, and

wherein in the first operation mode, each of the p-channel and n-channel MISFETs have characteristics is that a leak current flows through the source-drain path even when the voltage between the gate and the source is 0 volts,

wherein in the second operation mode, a second current between the first node and the second node is smaller than the first current when the voltage between the gate and the source of one of the p-channel MISFET and the n-channel MISFET is 0 volts for each of the plurality of complementary MISFETs.

54. A semiconductor device according to claim 53, further comprising a circuit for making the threshold voltage of the p-channel MISFETs be a first threshold voltage at the first operation mode or a second threshold voltage at the second operation mode and making the threshold voltage of the n-channel MISFETs be a third threshold voltage at the first operation mode or a fourth threshold voltage at the second operation mode.

55. A semiconductor device according to claim 54, wherein the first threshold voltage is larger than the second threshold voltage and the third threshold voltage is smaller than the fourth threshold voltage.

56. A semiconductor device according to claim 55, wherein the switching speed of the plurality of complementary MISFETs at the first operation mode is faster than that of the plurality of complementary MISFETs at the second operation mode.

57. A semiconductor device according to claim 53, wherein in the first operation mode, a leak current flowing through the source-drain path of each of the plurality of complementary MISFETs is about 1 μA when the voltage between the gate and the source of one of the p-channel MISFET and the n-channel MISFET is zero volt for each of the plurality of complementary MISFETs.

58. A semiconductor device according to claim 53,

wherein said semiconductor device is formed on a semiconductor substrate,

wherein the p-channel MISFETs of the plurality of complementary MISFETs are formed in a first semiconductor region with N-type,

wherein the N-channel MISFETs of the plurality of complementary MISFETs are formed in a second semiconductor region with P-type, and

wherein said semiconductor device further comprising a first voltage circuit for producing a first bias voltage supplied to the first semiconductor region and a second voltage circuit for producing a second bias voltage supplied to the second semiconductor region.

59. A semiconductor device according to claim 58,

wherein said semiconductor substrate has P-type,

wherein the second semiconductor region with P-type is isolated from the semiconductor substrate with P-type by a third semiconductor region with N-type, and

wherein the third semiconductor region is electrically connected to the first semiconductor region.

60. A semiconductor device according to claim 59,

wherein the first and second voltage circuit change the outputting voltage level depending on the first or second operation modes,

wherein the voltage of the first bias voltage at the first operation mode is lower than that of the first bias voltage at the second operation mode, and

wherein the voltage of the second bias voltage at the first operation mode is higher than that of the second bias voltage at the second operation mode.

61. A semiconductor device according to claim 60,

wherein the operating voltage is defined by a ground potential and a first potential higher than the ground potential, and

wherein the first bias voltage at the first operation is the first potential and the second bias voltage at the first operation mode is the ground potential.

62. A semiconductor device according to claim 59,

wherein the first voltage circuit includes a first oscillator and a first charge pumping circuit for generating the first bias voltage, and

wherein the second voltage circuit includes a second oscillator and a second charge pumping circuit for generating the second bias voltage.

63. A semiconductor device according to claim 58,

wherein the first operation mode is a high speed operation mode and the second operation mode is a low power consumption mode.

64. A semiconductor device according to claim 58, wherein the operating voltage is between 0.5V and 1.5V.

65. A semiconductor device according to claim 58, wherein said semiconductor device is an LSI chip including a microprocessor.

66. A semiconductor device comprising:

first circuit block including a first node, a second node, and a plurality of first complementary circuits, each having a P-channel MISFET and an N-channel MISFET connected in series between the first node and the second node,

a second circuit block including a third node, a fourth node, and a plurality of second complementary circuits, each having a P-channel MISFET and an N-channel MISFET connected in series between the third node and the fourth node,

wherein said semiconductor device has a first operation node and a second operation node,

wherein in the first operation mode an operating voltage is supplied between first and second nodes and an operating voltage is supplied between third and fourth nodes,

wherein in the second operation mode, no operating voltage is supplied between first and second nodes and an operating voltage is supplied between third and fourth nodes,

wherein in the first operation mode, a current between the first node and the second node flows through each of the plurality of complementary MISFETs when the voltage between the gate and the source of one of the P-channel MISFET and the N-channel MISFET is 0 volts for each of the plurality of complementary MISFETs, and

wherein in the first operation mode, each of the P-channel and N-channel MISFETs have characteristics that a leak current flows through the source-drain path even when the voltage between the gate and the source of 0 volts.

67. A semiconductor device according to claim 66, further comprising:

a first circuit for making the threshold voltage of the P-channel MISFETs of the plurality of second complementary circuits be a first threshold voltage at the first operation mode or a second threshold voltage at the second operation mode; and

a second circuit for making the threshold voltage of the N-channel MISFETs of the plurality of second complementary circuits be a third threshold voltage at the first operation mode or a fourth threshold voltage at the second operation mode.

68. A semiconductor device according to claim 67, wherein the first threshold voltage is larger than the second threshold voltage and the third threshold voltage is smaller than the fourth threshold voltage.

69. A semiconductor device according to claim 67, wherein the switching speed of the plurality of second complementary circuits at the first operation mode is faster than that of the plurality of second complementary circuits at the second operation mode.

70. A semiconductor device comprising:

a first circuit block including a first node, a second node, and a plurality of first complementary circuits, each having a P-channel first MISFET and an N-channel second MISFET connected in series between the first node and the second node,

a second circuit block including a third node, a fourth node, and a plurality of second complementary circuits, each having a P-channel third MISFET and an N-channel fourth MISFET connected in series between the third node and the fourth node,

wherein said semiconductor device has a first operation mode and a second operation mode,

wherein in the first operation mode, a first operating voltage is supplied between first and second nodes, a second operating voltage is supplied between third and fourth nodes, the threshold voltage of the P-channel third MISFETs is set to a first threshold voltage, and the threshold voltage of the N-channel fourth MISFETs is set to a second threshold voltage,

wherein in the second operation mode, no operating voltage is supplied between first and second nodes, the second operating voltage is supplied between third and fourth nodes, the threshold voltage of the P-channel third MISFETs is set to a third threshold voltage, and the threshold voltage of the N-channel fourth MISFETs is set to a fourth threshold voltage, wherein the first threshold voltage is larger than the second

threshold voltage and the third threshold voltage is smaller than the fourth threshold voltage.

71. A semiconductor device according to claim 70, wherein said semiconductor device is a semiconductor LSI chip including a memory circuit, and

wherein the second circuit block includes a circuit for keeping information stored in the memory.

72. A semiconductor device according to claim 70, wherein the first operation mode is a high speed operation node and the second operation mode is a low power consumption mode.

73. A semiconductor device according to claim 70, wherein the operating voltage is between 0.5V and 1.5V.

74. A semiconductor device according to claim 70, wherein in the first operation mode, each of the P-channel first MISFETs, the N-channel second MISFETs, the P-channel third MISFETs, and the N-channel fourth MISFETs have characteristics that a leak current flows through the source-drain path even when the voltage between the gate and the source is 0 volts.

REMARKS

Status of Claims

Applicants have canceled claims 1-52 and added claims 53-74. Claims 53-74 are the same as claims 72-93 of the parent reissue application, which were canceled without prejudice or disclaimer from the parent application under 37 C.F.R. 1.312(a).

Support for Claims Added by Amendment

Claims 53-74 are supported by Figs. 12A-15C. Fig. 15A shows complementary MISFETs including P-channel and N-channel MISFETs T_{33}, T_{32} and a circuit block 61 that also includes an operating voltage V_{CL2}. In a first operation mode, V_{P1} is at 0 volts. In the second operation mode, V_{BP1} is at -1 volts, as shown in Fig. 15C.

Claim 66 is supported by Fig. 15A, which shows a first circuit block 60 including P-channel and N-channel MISFETs T_{31} and T_{30}, respectively. In a first operation mode, shown in Fig. 15C, V_{BP1} equals 0 volts.

Claim 70 is also supported by Fig. 15A and includes first and second circuit blocks 60, 61. Support for the remainder of the claim is as discussed above with respect to claims 53 and 66.

Applicants request examination of the newly added claims in view of the foregoing remarks. Reconsideration and reexamination are respectfully requested.

Respectfully submitted,

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Date: May 25, 2001